

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:

09/903,059

Confirmation No.:

9375

First Named Inventor: Bulucea, Constantin

Filing Date:

10 July 2001

Group Art Unit:

2814

Examiner:

Farhani, D.

Atty. Docket No.:

NS-4971 US

Title:

Gate-Enhanced Junction Varactor

Assignee(s):

National Semiconductor Corporation

Mountain View, California 9 August 2004

COMMISSIONER FOR PATENTS PO Box 1450 Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT **UNDER 37 CFR 1.97(b)**

Sir:

2004-08-09 IDS.doc

Pursuant to 37 CFR 1.56, 1.97, and 1.98, each document listed on the accompanying substitute PTO Form 1449 is called to the attention of the Examiner for the above patent application. A copy of each listed document is enclosed.

Further enclosed is a copy of an English abstract of Japanese Patent Publication 4-199682.

Citation of each listed document shall not be construed as:

- 1. an admission that the document is necessarily prior art with respect to the instant invention;
- 2. a representation that a search has been made; or
- 3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

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Tel.: 650-964-9767 Fax: 650-964-9779 The preceding documents were cited during the prosecution of U.S. patent application 10/654,653 entitled "Gate-Enhanced Junction Varactor With Gradual Capacitance Variation".

This information disclosure statement is submitted under the provisions of 37 CFR 1.97(b).

EXPRESS MAIL LABEL NO.:

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Respectfully submitted,

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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | | | | | Applicant(s) | | | Confirmation No | |
| Substitute Form PTO 1449 | | | | | Bulucea, Constantin | | | 9375 | | |
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